CLAIMS

1. An address predecoder, comprising:

a decoder having input terminals for receiving column memory address signals and further having output terminals for providing initial predecode signals, the decoder selecting one of the output terminals on which to provide an active initial predecode signal based on the column memory address signals; and

a shifting circuit having inputs coupled to the output terminals of the decoder and control terminals for receiving shift control signals, the shifting circuit further having first and second sets of output terminals on which to provide respective column predecode signals, the shifting circuit providing first column predecode signals corresponding to the initial predecode signals on the first set of output terminals and, in response to receiving inactive shift control signals, providing second column predecode signals corresponding to the initial predecode signals and, in response to receiving active shift control signals, reordering the initial predecode signals into a shifted arrangement to be provided on the second set of output terminals as the second column predecode signals.

2. An address predecoder, comprising:

a decoder circuit having input terminals to receive address signals and further having output terminals to provide a plurality of predecode signals having logic levels that are determined by the address signals; and

a shifting circuit having input terminals coupled to the output terminals of the decoder circuit and a control terminal for receiving a shifting control signal, the shifting circuit further having a first set of output terminals to provide activation signals for accessing memory cells of a first memory cell array and a second set of output terminals to provide activation signals for accessing memory cells of a second memory cell array, the shifting circuit coupling each of the predecode signals to a respective one of the first set of the output terminals in

accordance with an arrangement determined by the shift control signal and coupling each of the predecode signals to a corresponding one of the second set of the output terminals.

3. The address predecoder of claim 2 wherein the first memory cell array is accessed for even memory addresses and the second memory cell array is access for odd memory addresses.

4. The address predecoder of claim 2 wherein the decoder circuit comprises a one-of-eight decoder having input terminals to receive three address signals.

5. The address predecoder of claim 2 wherein the decoder circuit selects only one of the output terminals on which to provide an active predecode signal in accordance with the address signals.

6. The predecoder of claim 2 wherein the shifting circuit, in response to accessing a starting memory location having an even memory address, couples the predecode signals to the first set of output terminals in the same arrangement as the predecode signals are coupled to the second set of output terminals.

7. The predecoder of claim 2 wherein the shifting circuit, in response to accessing a starting memory location having an odd memory address, couples the predecode signals to the first set of output terminals according to a first arrangement and couples the predecode signals to the second set of output terminals according to a second arrangement, the first arrangement having two signals transposed from the second arrangement.

8. An address predecoder, comprising:

a decoder circuit having input terminals for receiving input address signals and a plurality of output terminals for providing output signals in a predecode arrangement determined by input address signals; and

a shifting circuit having input terminals coupled to the output terminals of the decoder circuit and control terminals for receiving shift control signals, the shifting circuit having a first set of output terminals for providing a first set of activation signals in a first arrangement in accordance with the shift control signals and a second set of output terminals for providing a second set of activation signals in a second arrangement corresponding to the predecode arrangement.

9. The address predecoder of claim 8 wherein the shifting circuit provides the second set of activation signals in the second arrangement by coupling the predecode signals to the second output terminals in an arrangement different than coupling the predecode signals to the first output terminals.

10. The address predecoder of claim 8 wherein the decoder circuit comprises:

a plurality of latch circuits, each latch circuit having an input coupled to a respective input terminals of the decoder circuit and further having an output terminal at which to provide a latched address signal;

a plurality of inverters, each inverter having an input coupled to an output terminal of a respective latch circuit and further having an output;

a plurality of buffer circuits, each buffer circuit having an input coupled to an output terminal of a respective latch circuit and further having an output; and

a plurality of logic gates, each logic gate having input terminals coupled to a combination of outputs from the inverters and buffer circuits, no two logic gates having the same combination of input signals provided by the inverters and buffer circuits.

11. The address predecoder of claim 10 wherein each of the logic gates comprises a NAND gate.

12. The address predecoder of claim 10 wherein each of the logic gates comprises a NOR gate.

13. The address predecoder of claim 8 wherein the shifting circuit comprises a plurality of shifting blocks, each block having input terminals coupled to a portion of the output terminals of the decoder circuit and having shifting control terminals coupled to receive the shift control signals, each block further having first and second pairs of output terminals, the first pair providing two signals of the first set of activation signals and the second pair providing two signals of the second set of activation signals in accordance with the shift control signals.

14. The address predecoder of claim 13 wherein each shifting block comprises a plurality of transfer gates, each transfer gate having a control terminal coupled to receive a respective control signal and further having an input terminal coupled to receive a respective predecode signal, a first set of transfer gates for coupling one of the respective predecode signal to a first terminal of the second pair of output terminals and a second set of transfer gates coupling another one of the respective predecode signals to a second terminal of the second pair of output terminals.

15. The address predecoder of claim 14 wherein each shifting block further comprises a plurality of a pair of series coupled inverters, each pair of inverters having an output terminal coupled to a different output terminal of the shifting block.

16. An address predecoder, comprising:

a predecoder circuit receiving memory address bits and providing at output terminals an output value determined by the bits of the memory address; and

a shifting circuit having input terminals coupled to the output terminals of the predecoder circuit and a control terminal for receiving a shift control signal, the shifting circuit further having first and second sets of output terminals for providing a respective activation value, the first activation value equal to the output value of the predecoder and the second activation value determined by the shift control signal.

17. The address predecoder of claim 16 wherein the predecoder receives column memory address bits and the shifting circuit provides activation values for selecting columns of a memory to access.

18. The address predecoder of claim 16 wherein the predecoder receives column memory address bits and the shifting circuit provides activation values for additional decode to select columns of a memory to access.

19. An address predecoder circuit, comprising:

a decoder circuit having input terminals for receiving a memory address and further having output terminals for providing predecode signals, the decoder circuit selecting one of the output terminals to provide an active predecode signal based on the memory address; and

transfer gate circuitry coupled to the output terminals of the decoder circuit, the transfer gate circuitry having control terminals for receiving control signals and further having first and second sets of output terminals, each set of output terminals having a number of terminals equal to the number of output terminals of the decoder circuit, the transfer gate circuitry coupling the active predecode signal to a corresponding output terminal of the first set of output terminals and coupling the active predecode signal to one of the second set of output terminals based on the control signals.

20. The address predecoder circuit of claim 19 wherein the transfer gate circuitry couples the active predecode signal to a corresponding output terminal of the second set of output terminals.

21. The address predecoder circuit of claim 19 wherein the transfer gate circuitry comprises a plurality of transfer gate blocks, each transfer gate block having input terminals to receive three of the predecode signals and further having first and second pairs of output terminals, each transfer gate block coupling a first and a second of the three predecode signals to a first terminal and a second terminal of the first pair of output terminals, respectively, and

in response to receiving inactive control signals, the transfer gate block coupling the first and the second of the three predecode signals to a first terminal and a second terminal of the second pair of output terminals, respectively, and

in response to receiving active control signals, the transfer gate block coupling the second or third of the three predecode signals to the first terminal of the second pair of the output terminals and coupling the first of the predecode signals to the second terminal of the second pair of output terminals.

22. The address predecoder circuit of claim 21 wherein the transfer gate block couples the second of the three predecode signals to the first terminal of the second pair of the output terminals in response to receiving active control signals indicating accessing a first number of memory cells and the transfer gate block couples the third of the three predecode signals to the first terminal of the second pair of the output terminals in response to receiving active control signals indicating accessing a second number of memory cells.

23. A memory device, comprising:

at least one array of memory cells having first and second memory cell sub-arrays, the memory cells arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit coupled to the address bus for activating a row line corresponding to a row address coupled to the row address circuit through the address bus; and

a column address circuit coupled to the address bus for receiving an external column address and for selecting a column of the memory array corresponding to an internal column address, the column address circuit having an address predecoder, the address predecoder comprising:

a decoder circuit having input terminals coupled to receive the internal column addresses and further having output terminals to provide a plurality of predecode signals having logic levels that are determined by the internal column addresses; and

a shifting circuit having input terminals coupled to the output terminals of the decoder circuit and a control terminal for receiving a shifting control signal, the shifting circuit further having a first set of output terminals to provide activation signals for selecting a column of the first memory cell sub-array and a second set of output terminals to provide activation signals for selecting a column of the second memory cell sub-array, the shifting circuit coupling each of the predecode signals to a respective one of the first set of the output terminals in accordance with an arrangement determined by the shift control signal and coupling each of the predecode signals to a corresponding one of the second set of the output terminals.

24. The memory device of claim 23 wherein the first memory cell sub-array is accessed for even column addresses and the second memory cell sub-array is accessed for odd column addresses.

25. The memory device of claim 23 wherein the decoder circuit of the address predecoder comprises a one-of-eight decoder having input terminals to receive three address signals.

26. The memory device of claim 23 wherein the decoder circuit of the address predecoder selects only one of the output terminals on which to provide an active predecode signal in accordance with the address signals.

27. The memory device of claim 23 wherein the shifting control signals comprise signals that indicate the number of columns to access in response to receiving an external column address.

28. The memory device of claim 23 wherein the shifting circuit of the predecode circuit, in response to accessing a starting memory location having an even memory address, couples the predecode signals to the first set of output terminals in the same arrangement as the predecode signals are coupled to the second set of output terminals.

29. The memory device of claim 23 wherein the shifting circuit of the predecode circuit, in response to accessing a starting memory location having an odd memory address, couples the predecode signals to the first set of output terminals according to a first arrangement and couples the predecode signals to the second set of output terminals according to a second arrangement, the first arrangement having two signals transposed from the second arrangement.

30. A memory device, comprising:

at least one array of memory cells having first and second memory sub-arrays, the memory cells arranged in rows and columns, each of the rows having a row line and each of the columns having a pair of complementary digit lines;

a row address circuit coupled to the address bus for activating a row line corresponding to a row address coupled to the row address circuit through the address bus; and

a column address circuit coupled to the address bus for receiving an external column address and for selecting a column of the memory array corresponding to an internal column address, the column address circuit having an address predecoder, the address predecoder comprising:

a decoder circuit having input terminals coupled to receive internal column addresses and further having a plurality of output terminals for providing output signals in a predecode arrangement determined by the internal column addresses; and

a shifting circuit having input terminals coupled to the output terminals of the decoder circuit and control terminals for receiving shift control signals, the shifting circuit having first and second sets of output terminals, the shifting circuit providing from the first set of output terminals a first set of activation signals in a first arrangement corresponding to the predecode arrangement to access a column in the first memory sub-array and providing from the second set of output terminals a second set of activation signals in a second arrangement in accordance with the shift control signals to access a column in the second memory sub-array.

31. The memory device of claim 30 wherein the shifting circuit of the address predecoder provides the second set of activation signals in the second arrangement by coupling the predecode signals to the second output terminals in an arrangement different than coupling the predecode signals to the first output terminals.

32. The memory device of claim 30 wherein the decoder circuit of the address predecoder comprises:

a plurality of latch circuits, each latch circuit having an input coupled to a respective input terminals of the decoder circuit and further having an output terminal at which to provide a latched internal column address signal;

a plurality of inverters, each inverter having an input coupled to an output terminal of a respective latch circuit and further having an output;

a plurality of buffer circuits, each buffer circuit having an input coupled to an output terminal of a respective latch circuit and further having an output; and

a plurality of logic gates, each logic gate having input terminals coupled to a combination of outputs from the inverters and buffer circuits, no two logic gates having the same combination of input signals provided by the inverters and buffer circuits.

33. The memory device of claim 32 wherein each of the logic gates of the address predecoder comprises a NAND gate.

34. The memory device of claim 32 wherein each of the logic gates of the address predecoder comprises a NOR gate.

35. The memory device of claim 30 wherein the shifting circuit of the address predecoder comprises a plurality of shifting blocks, each block having input terminals coupled to a portion of the output terminals of the decoder circuit and having shifting control terminals coupled to receive the shift control signals, each block further having first and second pairs of output terminals, the first pair providing two signals of the first set of activation signals and the second pair providing two signals of the second set of activation signals in accordance with the shift control signals.

36. The memory device of claim 35 wherein each shifting block of the address predecoder comprises a plurality of transfer gates, each transfer gate having a control terminal coupled to receive a respective control signal and further having an input terminal coupled to receive a respective predecode signal, a first set of transfer gates for coupling one of the respective predecode signal to a first terminal of the second pair of output terminals and a second

set of transfer gates coupling another one of the respective predecode signals to a second terminal of the second pair of output terminals.

37. The memory device of claim 36 wherein each shifting block of the address predecoder further comprises a plurality of a pair of series coupled inverters, each pair of inverters having an output terminal coupled to a different output terminal of the shifting block.

38. A method for predecoding memory addresses, comprising:
generating a set of predecode signals having one active predecode signal;
coupling the predecode signals according to a first arrangement; and
coupling the predecode signals according to a second arrangement.

39. The method of claim 38 wherein coupling the predecode signals according to the second arrangement comprises switching the position of the active predecode signal with one of the remaining predecode signals of the first arrangement.

40. A method for predecoding a memory address, comprising:
generating a sequence of predecode signals based on the memory address;
providing the sequence of predecode signals as a first set of activation signals; and
based on the value of the memory address, either resequencing the sequence of predecode signals and providing the resequenced predecode signals as a second set of activation signals or providing the sequence of predecode signals as the second set of activation signals.

41. The method of claim 40, further comprising selecting a first column of memory according the first set of activation signals and selecting a second column of memory according to the second set of activation signals.

42. The method of claim 40 wherein generating a sequence of predecode signals comprises selecting one of the predecode signals to make active based on the memory address.

43. The method of claim 40 wherein resequencing the sequence of predecode signals and providing the resequenced predecode signals as a second set of activation signals comprises coupling the predecode signals to a set of output terminals in an order determined by control signals indicative of the number of memory cells to be accessed for the memory address.